LMV321/LMV358/LMV358-Q1/LMV358-Q3/LMV324 Single/Dual/Quad General Purpose, Low Voltage, Rail-to-Rail Output Operational Amplifiers

Check for Samples: LMV321-N, LMV358-N, LMV358-N-Q1, LMV358-N-Q3, LMV324-N

FEATURES

- (For $V^+ = 5V$ and $V^- = 0V$, unless otherwise specified)
- LMV358 is available in Automotive AEC-Q100 Grade 1 version
- Guaranteed 2.7V and 5V performance
- No crossover distortion
- Industrial temperature range −40°C to +125°C
- Gain-bandwidth product 1 MHz
- Low supply current
- LMV321 130 µA
- LMV358 210 µA
- LMV324 410 µA
- Rail-to-rail output swing @ 10 kΩ $V^+ - 10$ mV & $V^- + 65$ mV
- V_{CM} Range −0.2V to $V^+ - 0.8V$

APPLICATIONS

- Active filters
- General purpose low voltage applications
- General purpose portable devices

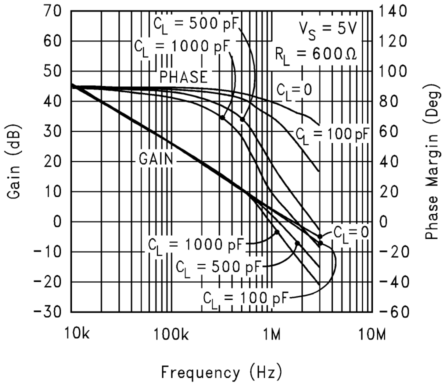
DESCRIPTION

The LMV358/LMV324 are low voltage (2.7V to 5.5V) versions of the dual and quad commodity op amps LM358/LM324 (5V to 30V). The LMV321 is the single channel version. The LMV321/LMV358/LMV324 are the most cost effective solutions for applications where low voltage operation, space efficiency, and low price are important. They offer specifications that meet or exceed the familiar LM358/LM324. The LMV321/LMV358/LMV324 have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed to power ratio, achieving 1 MHz of bandwidth and 1 V/µs slew rate with low supply current.

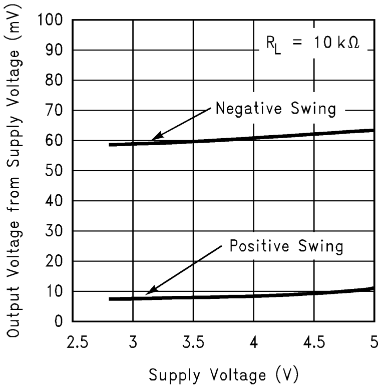
The LMV321 is available in the space saving 5-Pin SC70, which is approximately half the size of the 5-Pin SOT23. The small package saves space on PC boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with Texas Instruments's advanced submicron silicon-gate BiCMOS process. The LMV321/LMV358/LMV324 have bipolar input and output stages for improved noise performance and higher output current drive.

Gain and Phase vs. Capacitive Load



Output Voltage Swing vs. Supply Voltage



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	
Human Body Model	
LMV358/LMV324	2000V
LMV321	900V
Machine Model	100V
Differential Input Voltage	±Supply Voltage
Input Voltage	−0.3V to +Supply Voltage
Supply Voltage ($V^+–V^-$)	5.5V
Output Short Circuit to V^+	(4)
Output Short Circuit to V^-	(5)
Soldering Information	
Infrared or Convection (30 sec)	260°C
Storage Temp. Range	−65°C to 150°C
Junction Temperature (6)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC
(4) Shorting output to V^+ will adversely affect reliability.
(5) Shorting output to V^-will adversely affect reliability.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Supply Voltage	2.7V to 5.5V
Temperature Range (2)	
LMV321/LMV358/LMV324	−40°C to +125°C
Thermal Resistance (θ_{JA}) (3)	
5-pin SC70	478°C/W
5-pin SOT23	265°C/W
8-Pin SOIC	190°C/W
8-Pin MSOP	235°C/W
14-Pin SOIC	145°C/W
14-Pin TSSOP	155°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
(3) All numbers are typical, and apply for packages soldered directly onto a PC board in still air.

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			1.7	7	mV
TCV_{OS}	Input Offset Voltage Average Drift			5		µV/°C
I_B	Input Bias Current			11	250	nA
I_{OS}	Input Offset Current			5	50	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	50	63		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V	50	60		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0	−0.2		V
				1.9	1.7	V
V_O	Output Swing	R_L = 10 kΩ to 1.35V	V^+ −100	V^+ −10		mV
				60	180	mV
I_S	Supply Current	LMV321		80	170	µA
		LMV358 Both amplifiers		140	340	µA
		LMV324 All four amplifiers		260	680	µA

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
GBWP	Gain-Bandwidth Product	C_L = 200 pF		1		MHz
Φ_m	Phase Margin			60		Deg
G_m	Gain Margin			10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz		46		$\frac{nV}{\sqrt{Hz}}$ (1)
i_n	Input-Referred Current Noise	f = 1 kHz		0.17		$\frac{pA}{\sqrt{Hz}}$ (2)

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage			1.7	7 **9**	mV
TCV_{OS}	Input Offset Voltage Average Drift			5		μV/°C
I_B	Input Bias Current			15	250 **500**	nA
I_{OS}	Input Offset Current			5	50 **150**	nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	50	65		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V, V_{CM} = 1V	50	60		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0	−0.2		V
				4.2	4	V
A_V	Large Signal Voltage Gain (3)	R_L = 2 kΩ	15 **10**	100		V/mV
V_O	Output Swing	R_L = 2 kΩ to 2.5V	V^+ − 300 **V^+ − 400**	V^+ −40		mV
		R_L = 2 kΩ to 2.5V		120	300 **400**	
		R_L = 10 kΩ to 2.5V	V^+ − 100 **V^+ − 200**	V^+ − 10		mV
		R_L = 2 kΩ to 2.5V, 125°C		65	180 **280**	
I_O	Output Short Circuit Current	Sourcing, V_O = 0V	5	60		mA
		Sinking, V_O = 5V	10	160		
I_S	Supply Current	LMV321		130	250 **350**	μA
		LMV358 (both amps)		210	440 **615**	
		LMV324 (all four amps)		410	830 **1160**	

(1) All limits are guaranteed by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

(3) R_L is connected to V^-. The output voltage is 0.5V ≤ V_O ≤ 4.5V.

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (1)	Typ (2)	Max (1)	Units
SR	Slew Rate	(3)		1		V/μs
GBWP	Gain-Bandwidth Product	C_L = 200 pF		1		MHz
Φ_m	Phase Margin			60		Deg
G_m	Gain Margin			10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz		39		$\frac{nV}{\sqrt{Hz}}$ (3)
i_n	Input-Referred Current Noise	f = 1 kHz		0.21		$\frac{pA}{\sqrt{Hz}}$ (4)

(1) All limits are guaranteed by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(3) Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

CONNECTION DIAGRAM

5-Pin SC70/SOT23

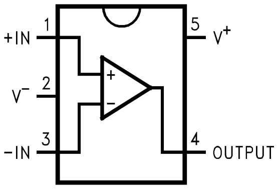


Figure 1. Top View

8-Pin SOIC/MSOP

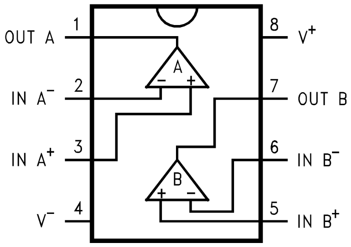


Figure 2. Top View

14-Pin SOIC/TSSOP

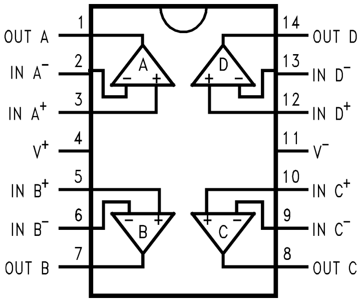


Figure 3. Top View

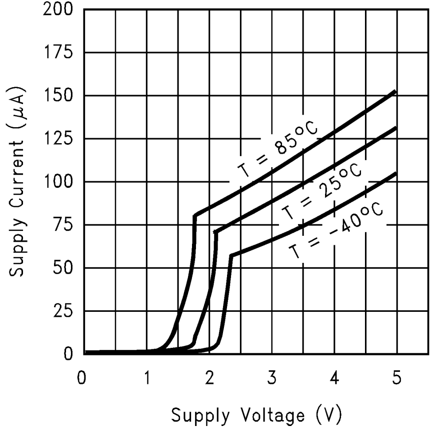
Devices with an asterisk (*) are future products. Please contact the factory for availability.

Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, includingdefect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. Fully compliant PPAP documentation is available.For more information go to http://www.national.com/automotive.

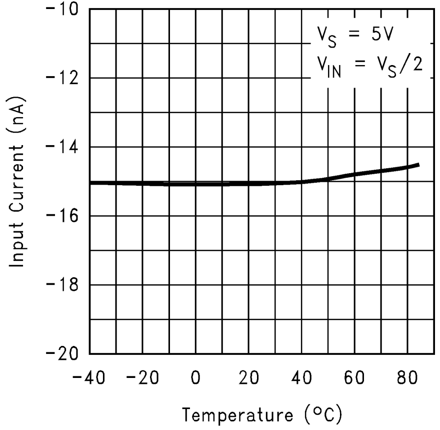
Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

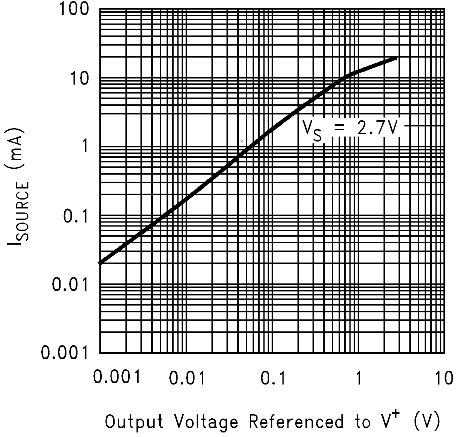
Supply Current vs. Supply Voltage (LMV321)



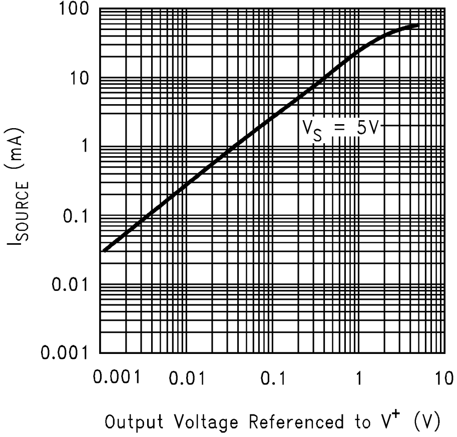
Input Current vs. Temperature



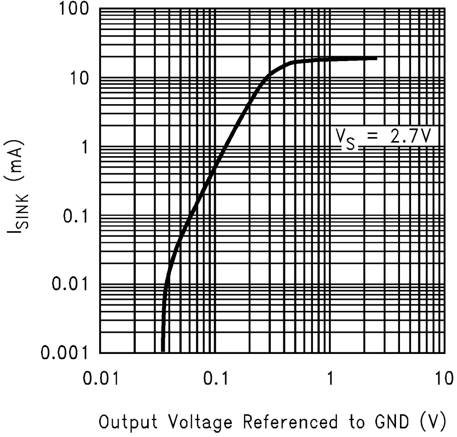
Sourcing Current vs. Output Voltage



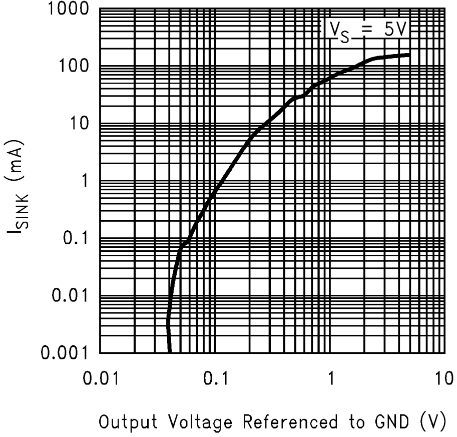
Sourcing Current vs. Output Voltage



Sinking Current vs. Output Voltage



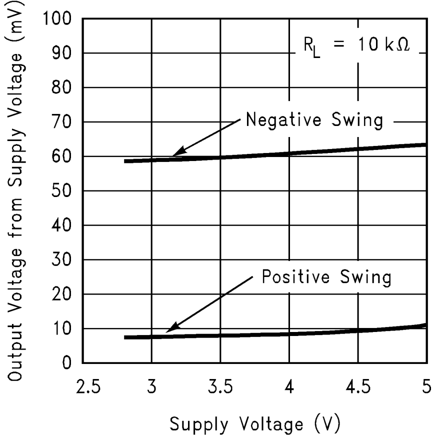
Sinking Current vs. Output Voltage



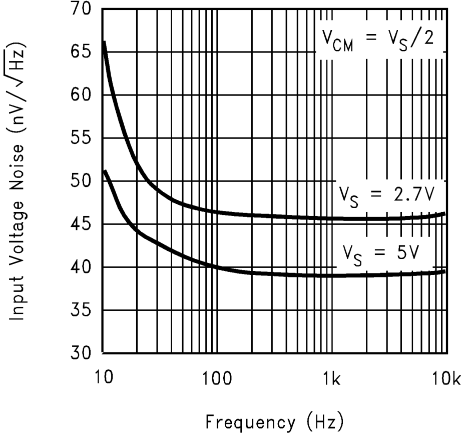
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

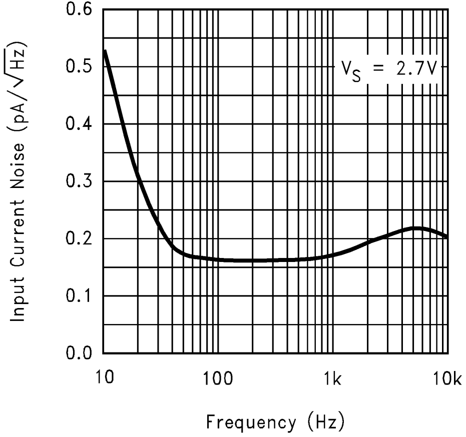
Output Voltage Swing vs. Supply Voltage



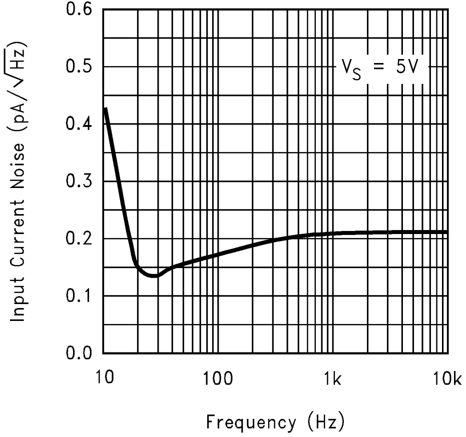
Input Voltage Noise vs. Frequency



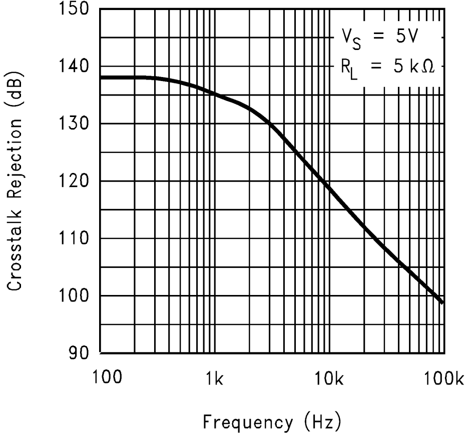
Input Current Noise vs. Frequency



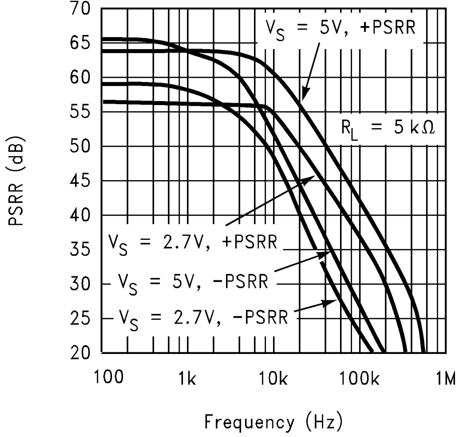
Input Current Noise vs. Frequency



Crosstalk Rejection vs. Frequency



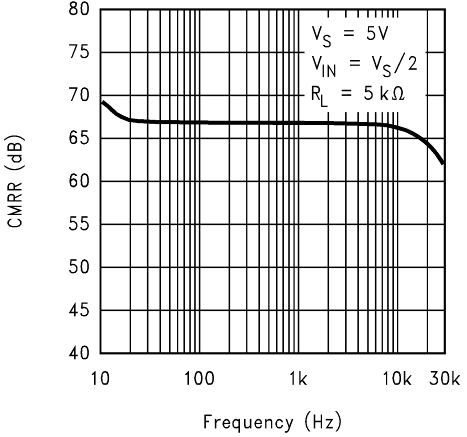
PSRR vs. Frequency



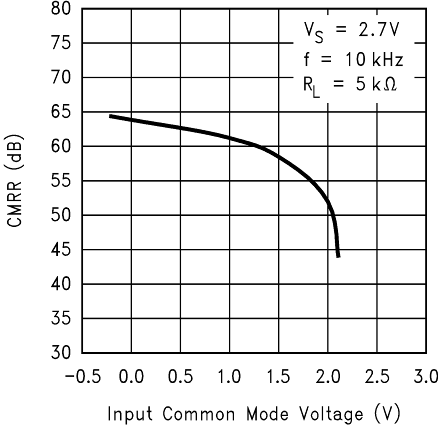
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

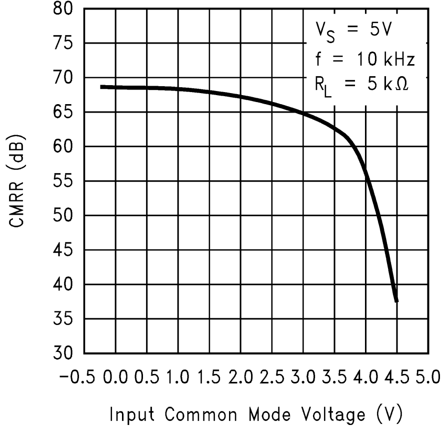
CMRR
vs.
Frequency



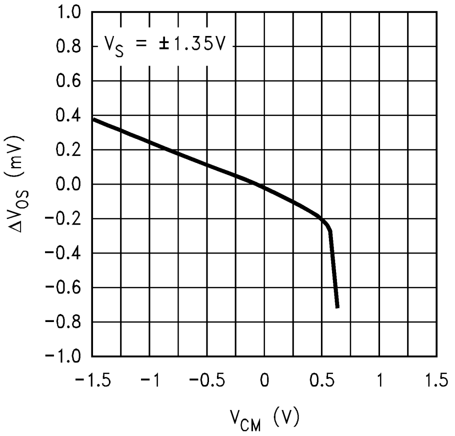
CMRR
vs.
Input Common Mode Voltage



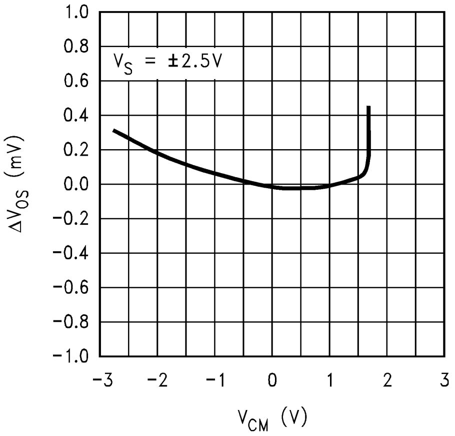
CMRR
vs.
Input Common Mode Voltage



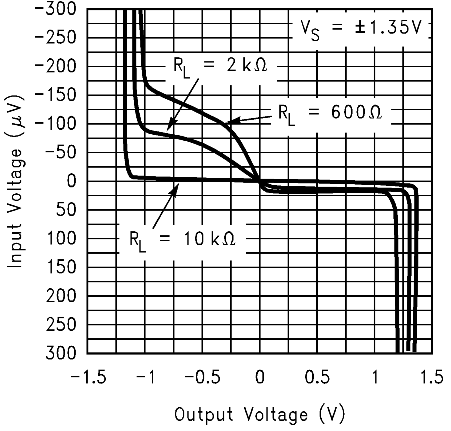
ΔV_{OS}
vs.
CMR



ΔV_{OS}
vs.
CMR



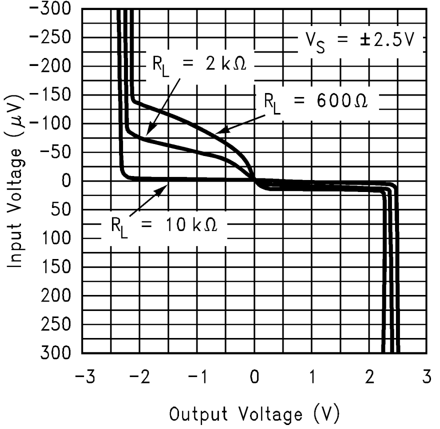
Input Voltage
vs.
Output Voltage



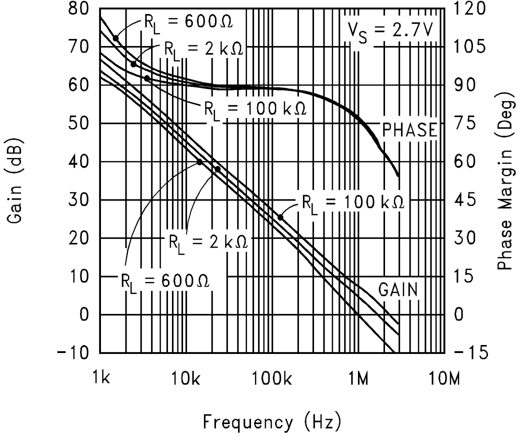
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

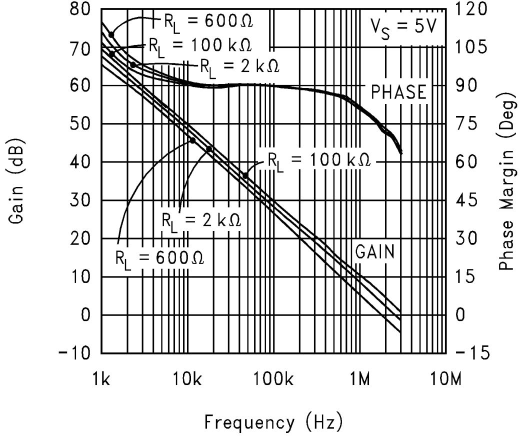
Input Voltage vs. Output Voltage



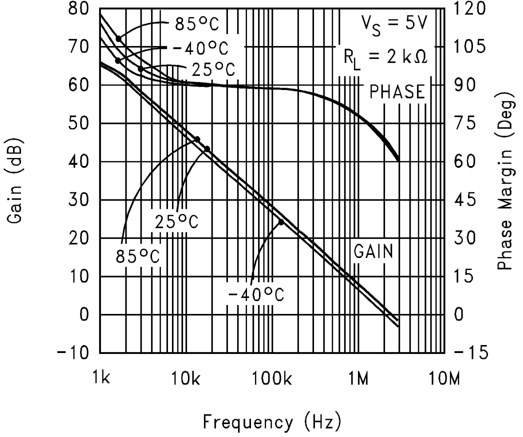
Open Loop Frequency Response



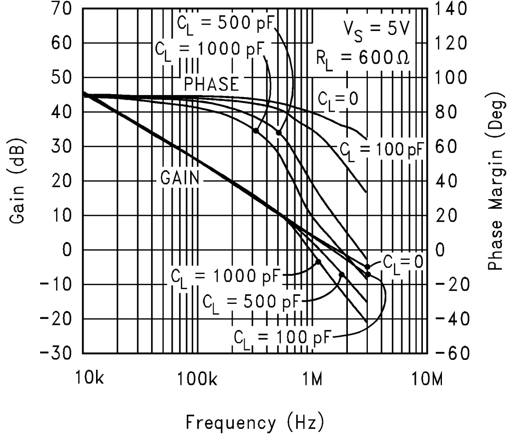
Open Loop Frequency Response



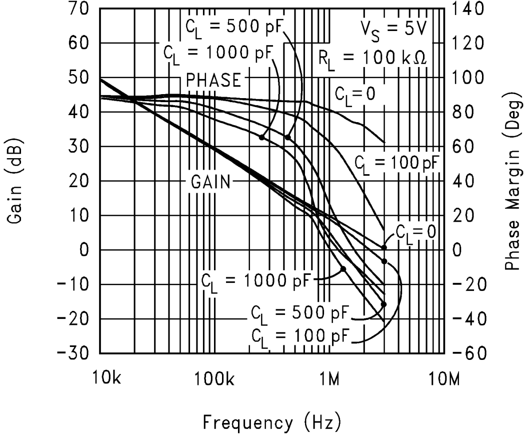
Open Loop Frequency Response vs. Temperature



Gain and Phase vs. Capacitive Load



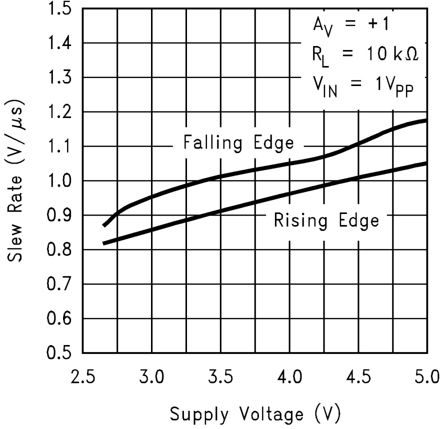
Gain and Phase vs. Capacitive Load



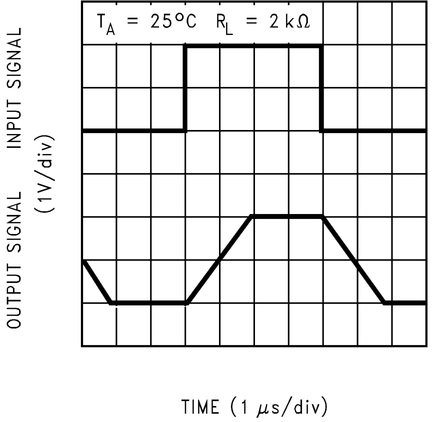
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

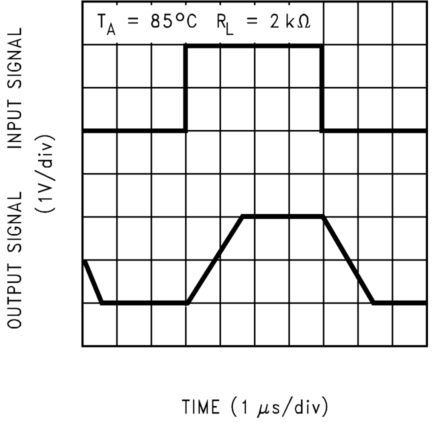
Slew Rate vs. Supply Voltage



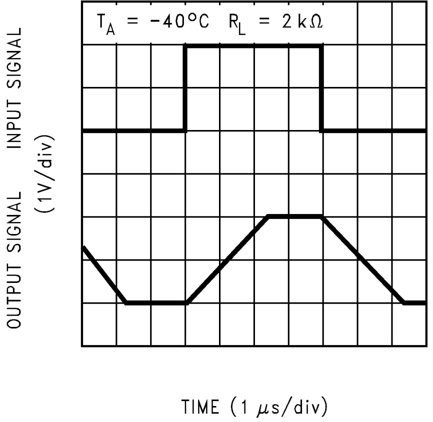
Non-Inverting Large Signal Pulse Response



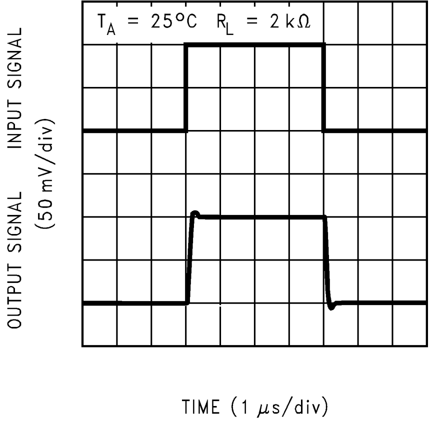
Non-Inverting Large Signal Pulse Response



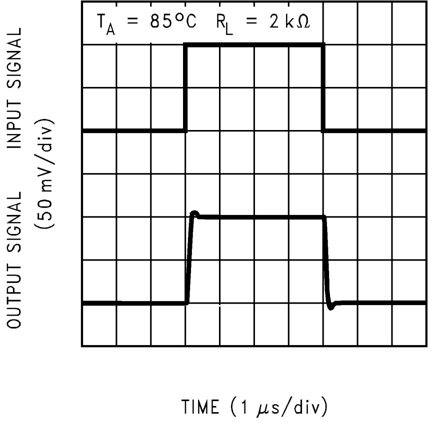
Non-Inverting Large Signal Pulse Response



Non-Inverting Small Signal Pulse Response



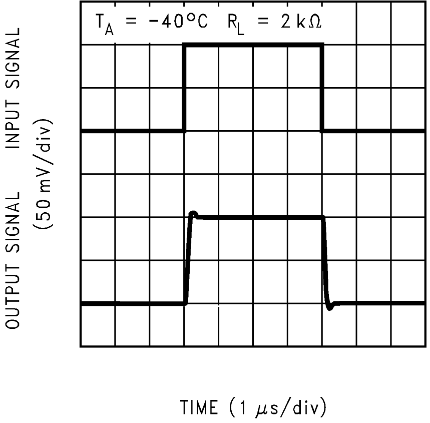
Non-Inverting Small Signal Pulse Response



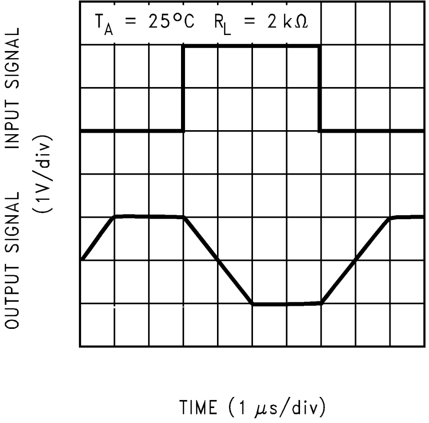
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

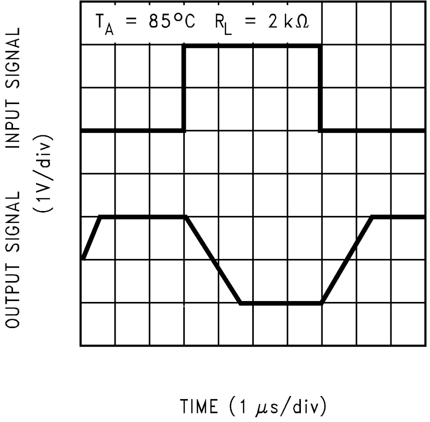
Non-Inverting Small Signal Pulse Response



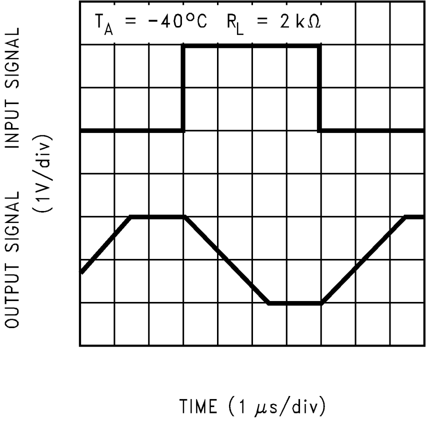
Inverting Large Signal Pulse Response



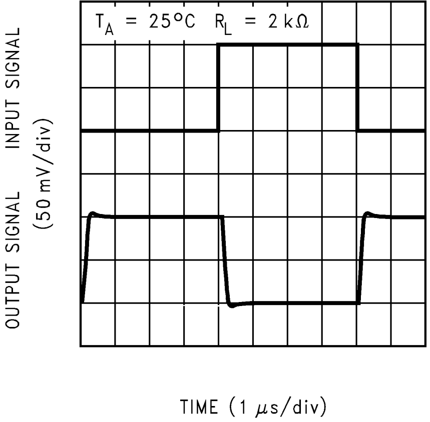
Inverting Large Signal Pulse Response



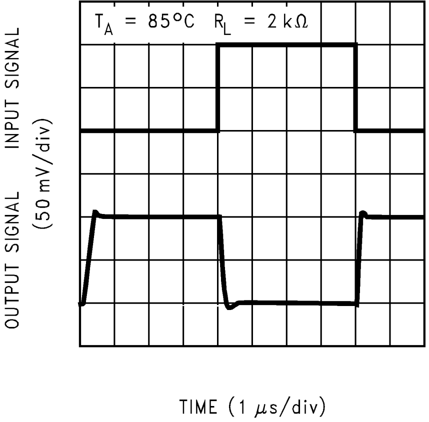
Inverting Large Signal Pulse Response



Inverting Small Signal Pulse Response

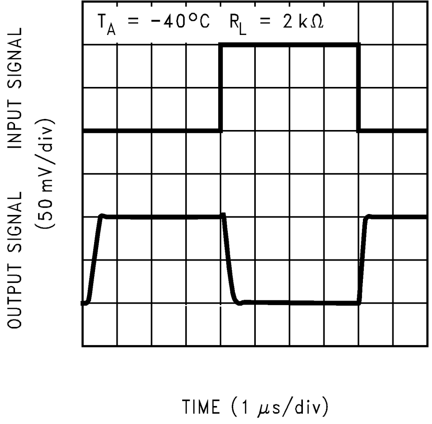


Inverting Small Signal Pulse Response

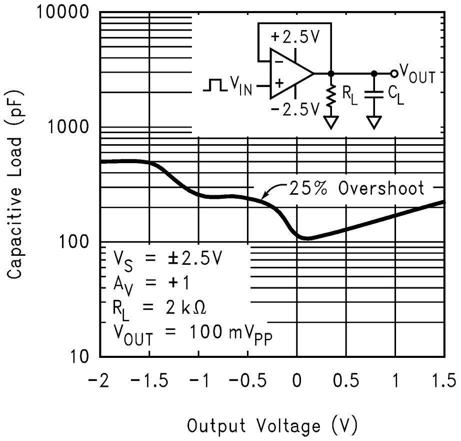


Typical Performance Characteristics (continued)

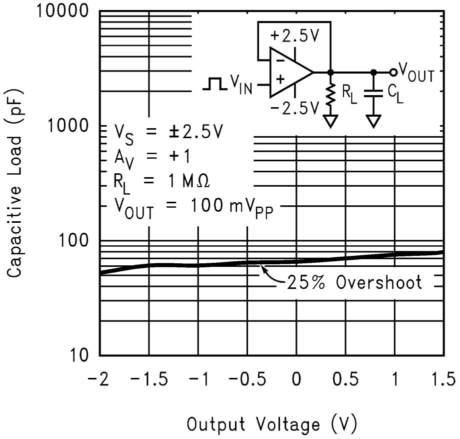
Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.



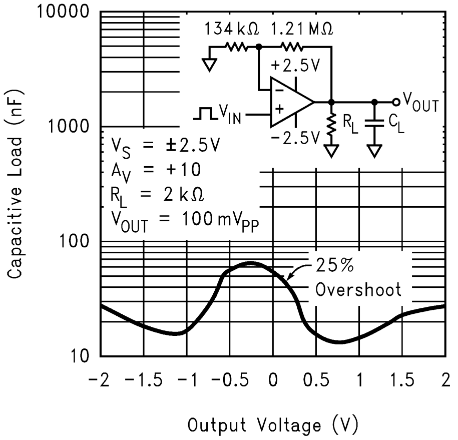
Inverting Small Signal Pulse Response



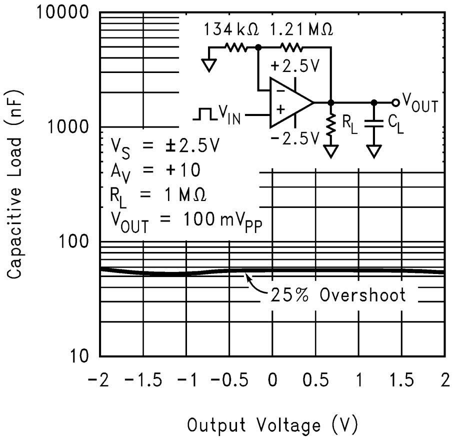
Stability vs. Capacitive Load



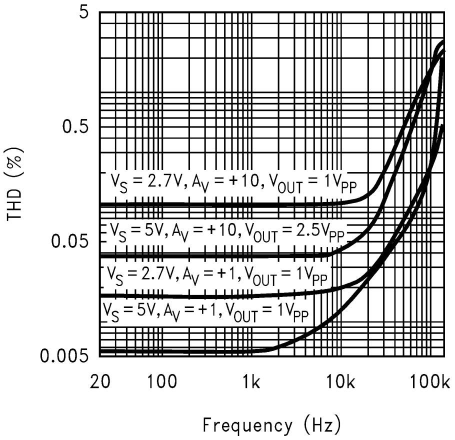
Stability vs. Capacitive Load



Stability vs. Capacitive Load



Stability vs. Capacitive Load

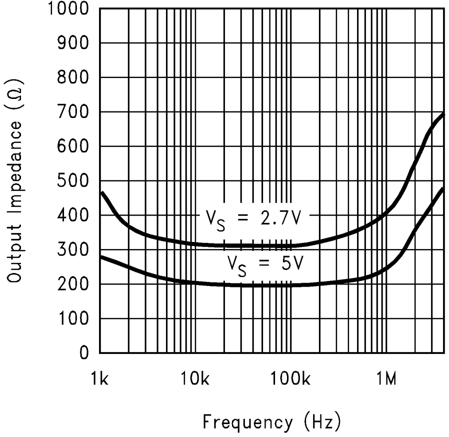


THD vs. Frequency

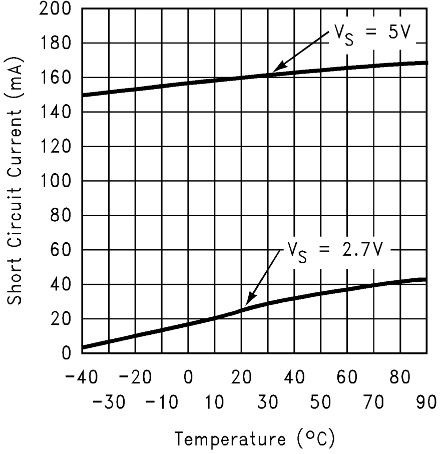
Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

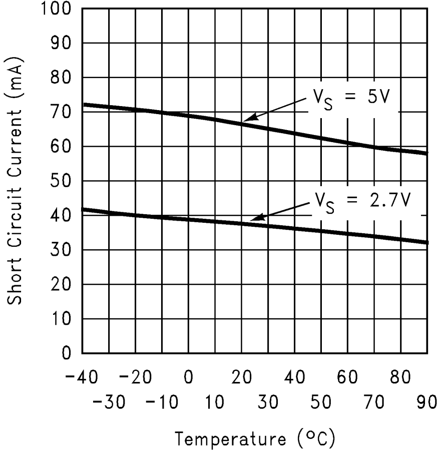
Open Loop Output Impedance vs. Frequency



Short Circuit Current vs. Temperature (Sinking)



Short Circuit Current vs. Temperature (Sourcing)



APPLICATION INFORMATION

BENEFITS OF THE LMV321/LMV358/LMV324

Size

The small footprints of the LMV321/LMV358/LMV324 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LMV321/LMV358/LMV324 make them possible to use in PCMCIA type III cards.

Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LMV321/LMV358/LMV324 can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

Simplified Board Layout

These products help you to avoid using long PC traces in your PC board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long PC traces.

Low Supply Current

These devices will help you to maximize battery life. They are ideal for battery powered systems.

Low Supply Voltage

Texas Instruments provides guaranteed performance at 2.7V and 5V. These guarantees ensure operation throughout the battery lifetime.

Rail-to-Rail Output

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Input Includes Ground

Allows direct sensing near GND in single supply operation.

Protection should be provided to prevent the input voltages from going negative more than −0.3V (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

Ease of Use and Crossover Distortion

The LMV321/LMV358/LMV324 offer specifications similar to the familiar LM324. In addition, the new LMV321/LMV358/LMV324 effectively eliminate the output crossover distortion. The scope photos in Figure 4 and Figure 5 compare the output swing of the LMV324 and the LM324 in a voltage follower configuration, with V_S = ± 2.5V and R_L (= 2 kΩ) connected to GND. It is apparent that the crossover distortion has been eliminated in the new LMV324.

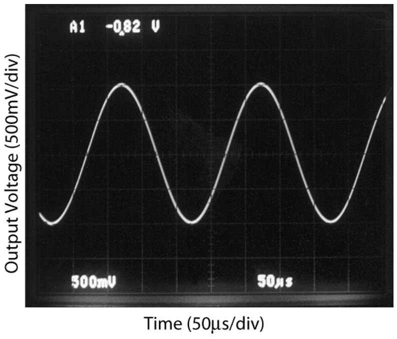


Figure 4. Output Swing of LMV324

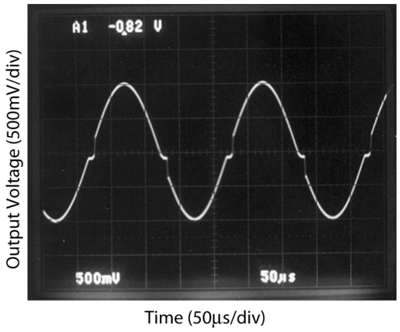


Figure 5. Output Swing of LM324

CAPACITIVE LOAD TOLERANCE

The LMV321/LMV358/LMV324 can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in Figure 6 can be used.

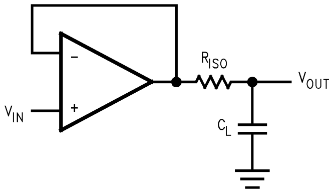


Figure 6. Indirectly Driving a Capacitive Load Using Resistive Isolation

In Figure 6 , the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Figure 7 is an output waveform of Figure 6 using 620Ω for R_{ISO} and 510 pF for C_L.

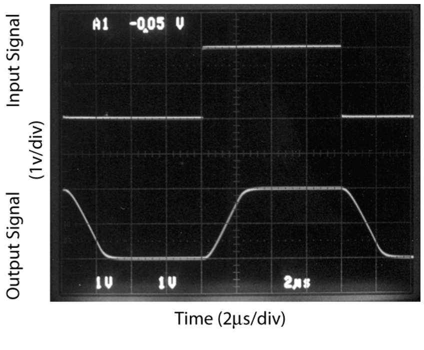


Figure 7. Pulse Response of the LMV324 Circuit in Figure 6

The circuit in Figure 8 is an improvement to the one in Figure 6 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 6, the output would be voltage divided by R_{ISO} and the load resistor. Instead, in Figure 8, R_F provides the DC accuracy by using feed-forward techniques to connect V_{IN} to R_L. Caution is needed in choosing the value of R_F due to the input bias current of theLMV321/LMV358/LMV324. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of C_F . This in turn will slow down the pulse response.

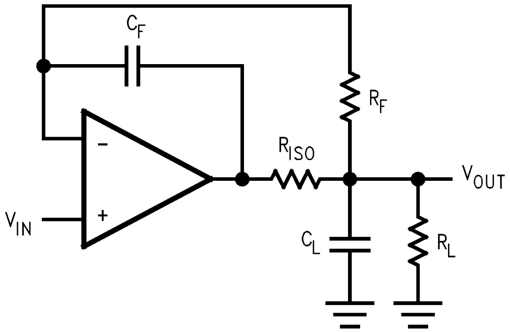


Figure 8. Indirectly Driving A Capacitive Load with DC Accuracy

INPUT BIAS CURRENT CANCELLATION

The LMV321/LMV358/LMV324 family has a bipolar input stage. The typical input bias current of LMV321/LMV358/LMV324 is 15 nA with 5V supply. Thus a 100 kΩ input resistor will cause 1.5 mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in Figure 9 shows how to cancel the error caused by input bias current.

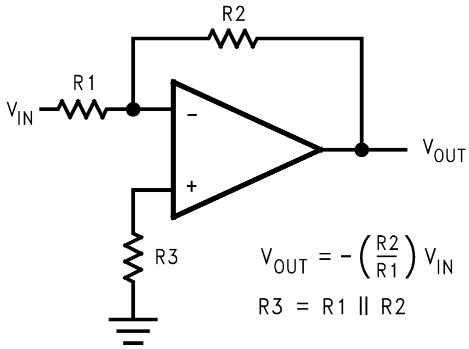
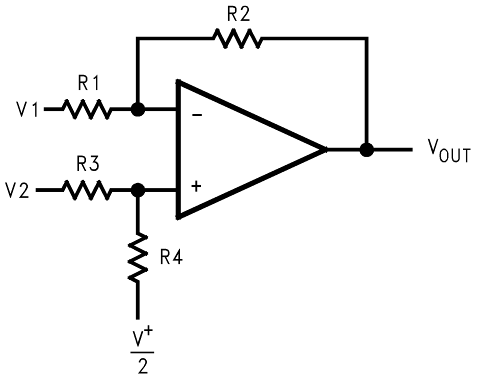


Figure 9. Cancelling the Error Caused by Input Bias Current

TYPICAL SINGLE-SUPPLY APPLICATION CIRCUITS

Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.



$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1 + \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R3}{R1} \bullet \frac{V^+}{2}$$

for R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}\left(V_2 - V_1\right) + \frac{V^+}{2}$$

Figure 10. Difference Amplifier

Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistors R_1, R_2, R_3, and R_4. To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

Three-Op-Amp Instrumentation Amplifier

The quad LMV324 can be used to build a three-op-amp instrumentation amplifier as shown in Figure 11.

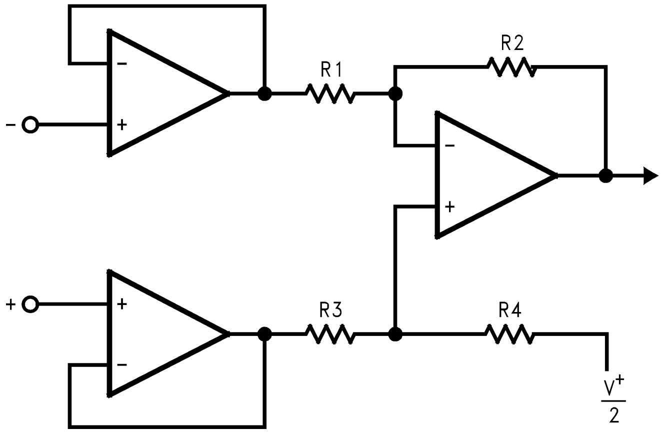
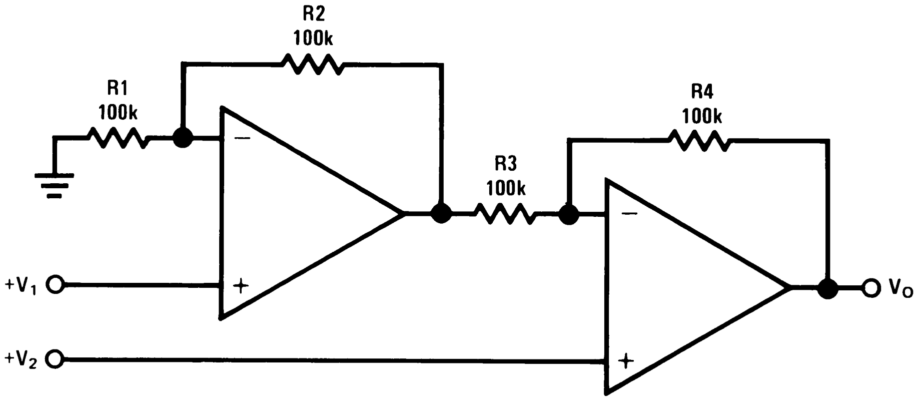


Figure 11. Three-Op-Amp Instrumentation Amplifier

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of R_2/R_1. R_3 should equal R_1, and R_4 equal R_2. Matching of R_3 to R_1 and R_4 to R_2 affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making R_4 slightly smaller than R_2 and adding a trim pot equal to twice the difference between R_2 and R_4 will allow the CMRR to be adjusted for optimum performance.

Two-Op-Amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance DC differential amplifier (Figure 12). As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. R_4 should equal R_1 and, R_3 should equal R_2.



$$V_O = \left(1 + \frac{R4}{R3}\right)(V_2 - V_1),\ \text{where } R1 = R4 \text{ and } R2 = R3$$

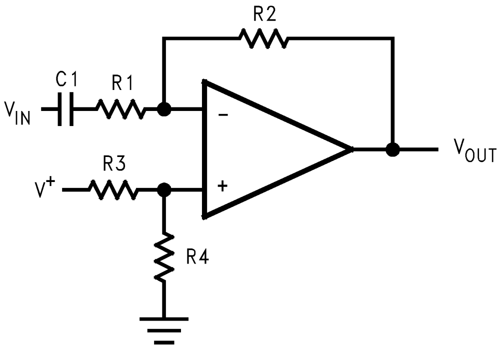
$$\text{As shown: } V_O = 2(V_2 - V_1)$$

Figure 12. Two-Op-Amp Instrumentation Amplifier

Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using R_3 and R_4 is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor C_1 is placed between the inverting input and resistor R_1 to block the DC signal going into the AC signal source, V_{IN}. The values of R_1 and C_1 affect the cutoff frequency, fc = $1/2\pi R_1 C_1$.

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.



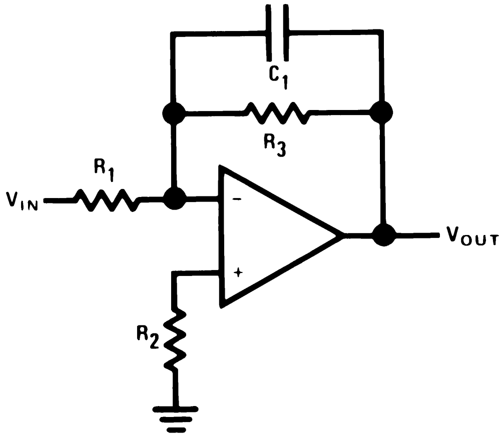
$$V_{OUT} = -\frac{R2}{R1} V_{IN}$$

Figure 13. Single-Supply Inverting Amplifier

ACTIVE FILTER

Simple Low-Pass Active Filter

The simple low-pass filter is shown in Figure 14. Its low-frequency gain (ω → 0) is defined by $-R_3/R_1$. This allows low-frequency gains other than unity to be obtained. The filter has a −20 dB/decade roll-off after its corner frequency fc. R_2 should be chosen equal to the parallel combination of R_1 and R_3 to minimize errors due to bias current. The frequency response of the filter is shown in Figure 15.



$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \,||\, R_3$$

Figure 14. Simple Low-Pass Active Filter

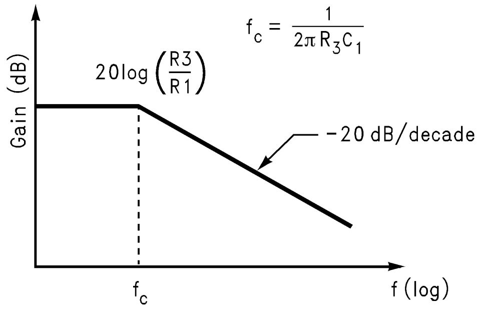


Figure 15. Frequency Response of Simple Low-Pass Active Filter in Figure 11

Note that the single-op-amp active filters are used in the applications that require low quality factor, Q(≤ 10), low frequency (≤ 5 kHz), and low gain (≤ 10), or a small value for the product of gain times Q (≤ 100). The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

$$\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6}\ \text{V}/\mu\text{sec} \tag{5}$$

where ω_H is the highest frequency of interest, and V_{OPP} is the output peak-to-peak voltage.

Sallen-Key 2nd-Order Active Low-Pass Filter

The Sallen-Key 2nd-order active low-pass filter is illustrated in Figure 16. The DC gain of the filter is expressed as

$$A_{LP} = \frac{R_3}{R_4} + 1 \tag{6}$$

Its transfer function is

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{\frac{1}{C_1 C_2 R_1 R_2} A_{LP}}{S^2 + S\left(\frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2}\right) + \frac{1}{C_1 C_2 R_1 R_2}} \quad (7)$$

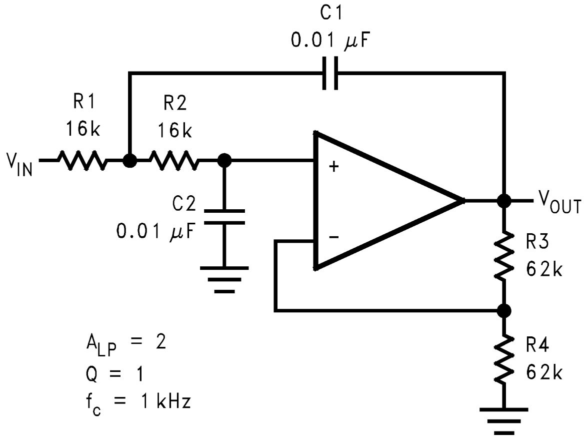


Figure 16. Sallen-Key 2nd-Order Active Low-Pass Filter

The following paragraphs explain how to select values for R_1, R_2, R_3, R_4, C_1, and C_2 for given filter requirements, such as A_{LP}, Q, and f_c.

The standard form for a 2nd-order low pass filter is

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{A_{LP}\,\omega_c^2}{S^2 + \left(\frac{\omega_c}{Q}\right)S + \omega_c^2} \quad (8)$$

where

Q: Pole Quality Factor

ω_C: Corner Frequency

A comparison between Equation 7 and Equation 8 yields

$$\omega_c^2 = \frac{1}{C_1 C_2 R_1 R_2} \quad (9)$$

$$\frac{\omega_c}{Q} = \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2} \quad (10)$$

To reduce the required calculations in filter design, it is convenient to introduce normalization into the components and design parameters. To normalize, let $\omega_C = \omega_n = 1$ rad/s, and $C_1 = C_2 = C_n = 1$F, and substitute these values into Equation 9 and Equation 10. From Equation 9, we obtain

$$R_1 = \frac{1}{R_2} \quad (11)$$

From Equation 10, we obtain

$$R_2 = \frac{1 \pm \sqrt{1 - 4Q^2(2 - A_{LP})}}{2Q} \quad (12)$$

For minimum DC offset, $V^+ = V^-$, the resistor values at both inverting and non-inverting inputs should be equal, which means

$$R_1 + R_2 = \frac{R_3 R_4}{R_3 + R_4} \quad (13)$$

From Equation 6 and Equation 13, we obtain

$$R_3 = (R_1 + R_2)A_{LP} \tag{14}$$

$$R_4 = \left(\frac{A_{LP}}{A_{LP}-1}\right)(R_1 + R_2) \tag{15}$$

The values of C_1 and C_2 are normally close to or equal to

$$C = \frac{10}{f_c}\mu F \tag{16}$$

As a design example:

Require: $A_{LP} = 2$, $Q = 1$, $fc = 1$ kHz

Start by selecting C_1 and C_2. Choose a standard value that is close to

$$C = \frac{10}{f_c}\mu F \tag{17}$$

$$C_1 = C_2 = \frac{10}{1 \times 10^3}\mu F = 0.01\ \mu F \tag{18}$$

From Equation 11 Equation 12 Equation 14 Equation 15,

R_1= 1Ω (19)
R_2= 1Ω (20)
R_3= 4Ω (21)
R_4= 4Ω (22)

The above resistor values are normalized values with $\omega_n = 1$ rad/s and $C_1 = C_2 = C_n = 1F$. To scale the normalized cutoff frequency and resistances to the real values, two scaling factors are introduced, frequency scaling factor (k_f) and impedance scaling factor (k_m).

$$k_f = \frac{\omega_c}{\omega_n} = \frac{2\pi \times 1 \times 10^3}{1} = 2\pi \times 10^3$$

$$k_m k_f = \frac{Cn}{C1}$$

$$k_m = 1.59 \times 10^4 \tag{23}$$

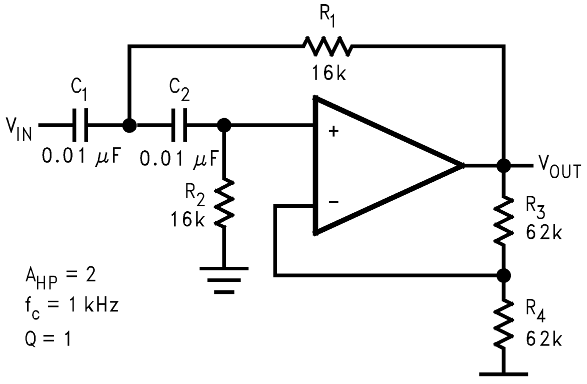
Scaled values:

$R_2 = R_1$ = 15.9 kΩ (24)
$R_3 = R_4$ = 63.6 kΩ (25)
$C_1 = C_2$ = 0.01 µF (26)

An adjustment to the scaling may be made in order to have realistic values for resistors and capacitors. The actual value used for each component is shown in the circuit.

2nd-Order High Pass Filter

A 2nd-order high pass filter can be built by simply interchanging those frequency selective components (R_1, R_2, C_1, C_2) in the Sallen-Key 2nd-order active low pass filter. As shown in Figure 17, resistors become capacitors, and capacitors become resistors. The resulted high pass filter has the same corner frequency and the same maximum gain as the previous 2nd-order low pass filter if the same components are chosen.


R1
16k
C1
C2
VIN
0.01 µF
0.01 µF
+
–
VOUT
R2
16k
R3
62k
R4
62k
AHP = 2
fc = 1 kHz
Q = 1

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{S^2 A_{HP}}{S^2 + S\left(\frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} + \frac{(1 - A_{HP})}{C_1 R_1}\right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

$$\text{Where } A_{HP} = 1 + \frac{R_3}{R_4}$$

Figure 17. Sallen-Key 2nd-Order Active High-Pass Filter

State Variable Filter

A state variable filter requires three op amps. One convenient way to build state variable filters is with a quad op amp, such as the LMV324 (Figure 18).

This circuit can simultaneously represent a low-pass filter, high-pass filter, and bandpass filter at three different outputs. The equations for these functions are listed below. It is also called "Bi-Quad" active filter as it can produce a transfer function which is quadratic in both numerator and denominator.

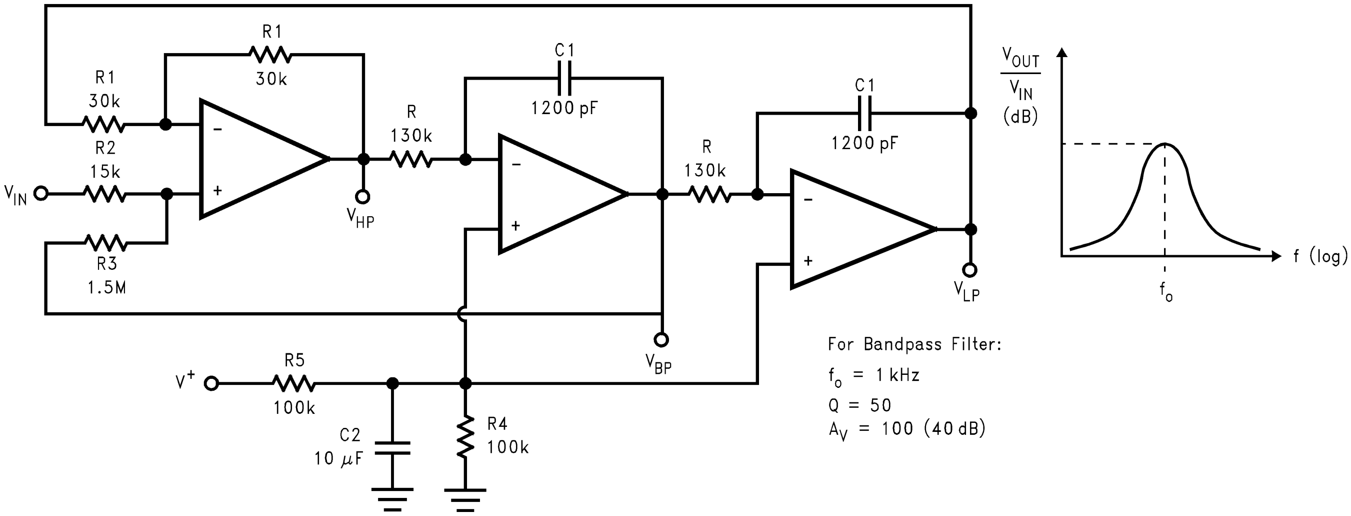

R1
30k
R1
30k
R2
15k
VIN
R3
1.5M
–
+
VHP
R
130k
C1
1200 pF
–
+
R
130k
VBP
C1
1200 pF
–
+
VLP
V+
R5
100k
C2
10 µF
R4
100k
For Bandpass Filter:
fo = 1 kHz
Q = 50
AV = 100 (40 dB)
VOUT / VIN (dB)
f (log)
fo

Figure 18. State Variable Active Filter

$$V_{LP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{\frac{1}{R^2C^2}}{S^2 + \frac{1}{\left(\frac{R_2 + R_3}{2R_2}\right) RC} S + \frac{1}{R^2C^2}} V_{IN}$$

$$V_{HP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{S^2}{S^2 + \frac{1}{\left(\frac{R_2 + R_3}{2R_2}\right) RC} S + \frac{1}{R^2C^2}} V_{IN}$$

$$V_{BP} = \left(\frac{2R_3}{R_2 + R_3}\right) \frac{\left(\frac{1}{RC}\right) S}{S^2 + \frac{1}{\left(\frac{R_2 + R_3}{2R_2}\right) RC} S + \frac{1}{R^2C^2}} V_{IN} \tag{27}$$

where for all three filters,

$$Q = \frac{R_2 + R_3}{2R_2} \tag{28}$$

$$\omega_0 = \frac{1}{RC} \quad \text{(resonant frequency)} \tag{29}$$

A design example for a bandpass filter is shown below:

Assume the system design requires a bandpass filter with f_O = 1 kHz and Q = 50. What needs to be calculated are capacitor and resistor values.

First choose convenient values for C_1, R_1 and R_2:

$$C_1 = 1200 \text{ pF} \tag{30}$$

$$2R_2 = R_1 = 30 \text{ k}\Omega \tag{31}$$

Then from Equation 28,

$$\begin{aligned} R_3 &= R_2(2Q-1) \\ R_3 &= 15\text{ k}\Omega \times (2 \times 50 - 1) \\ &= 1.5\text{ M}\Omega \end{aligned} \tag{32}$$

From Equation 29,

$$\begin{aligned} R &= \frac{1}{\omega_0 C_1} \\ R &= \frac{1}{(2\pi \times 10^3)(1.2 \times 10^{-9})} \\ &= 132.7\text{ k}\Omega \end{aligned} \tag{33}$$

From the above calculated values, the midband gain is $H_0 = R_3/R_2$ = 100 (40 dB). The nearest 5% standard values have been added to Figure 18.

PULSE GENERATORS AND OSCILLATORS

A pulse generator is shown in Figure 19. Two diodes have been used to separate the charge and discharge paths to capacitor C.

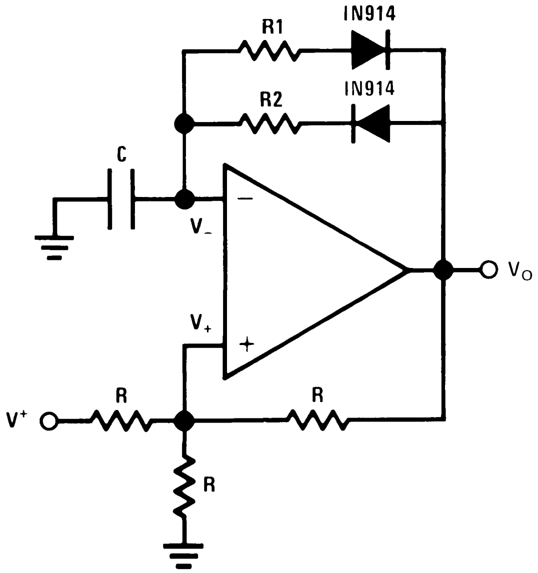
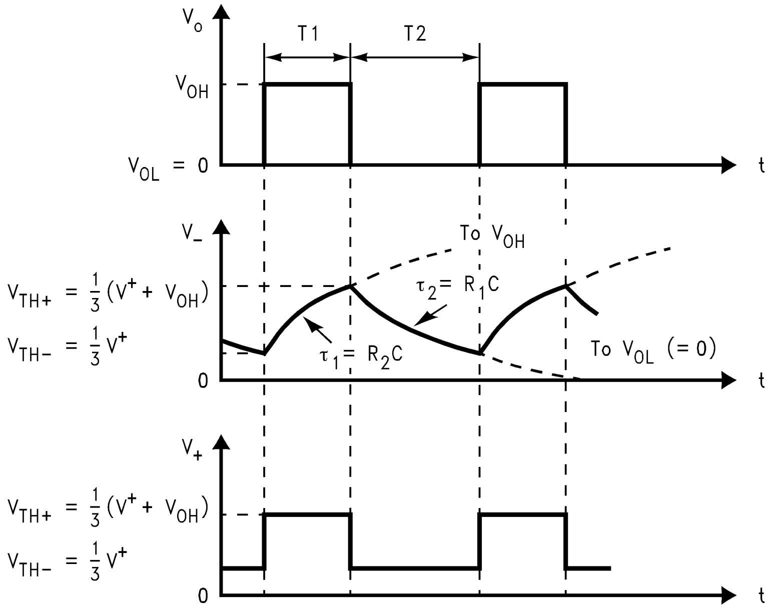


Figure 19. Pulse Generator

When the output voltage V_O is first at its high, V_{OH}, the capacitor C is charged toward V_{OH} through R_2. The voltage across C rises exponentially with a time constant $\tau = R_2C$, and this voltage is applied to the inverting input of the op amp. Meanwhile, the voltage at the non-inverting input is set at the positive threshold voltage (V_{TH+}) of the generator. The capacitor voltage continually increases until it reaches V_{TH+}, at which point the output of the generator will switch to its low, V_{OL} which 0V is in this case. The voltage at the non-inverting input is switched to the negative threshold voltage (V_{TH-}) of the generator. The capacitor then starts to discharge toward V_{OL} exponentially through R_1, with a time constant $\tau = R_1C$. When the capacitor voltage reaches V_{TH-}, the output of the pulse generator switches to V_{OH}. The capacitor starts to charge, and the cycle repeats itself.



$$T_1 = R_2C \ln \frac{3V_{OH} - V_{OL} - V^+}{2V_{OH} - V^+} \quad \text{and} \quad T_2 = R_1C \ln \frac{3V_{OL} - V_{OH} - V^+}{2V_{OL} - V^+}$$

When $V_{OL} = 0V$

$$T_1 = R_2C \ln \frac{3V_{OH} - V^+}{2V_{OH} - V^+} \quad \text{and} \quad T_2 = R_1C \ln \left(1 + \frac{V_{OH}}{V^+}\right)$$

Figure 20. Waveforms of the Circuit in Figure 16

As shown in the waveforms in Figure 20, the pulse width (T_1) is set by R_2, C and V_{OH}, and the time between pulses (T_2) is set by R_1, C and V_{OL}. This pulse generator can be made to have different frequencies and pulse width by selecting different capacitor value and resistor values.

Figure 21 shows another pulse generator, with separate charge and discharge paths. The capacitor is charged through R_1 and is discharged through R_2.

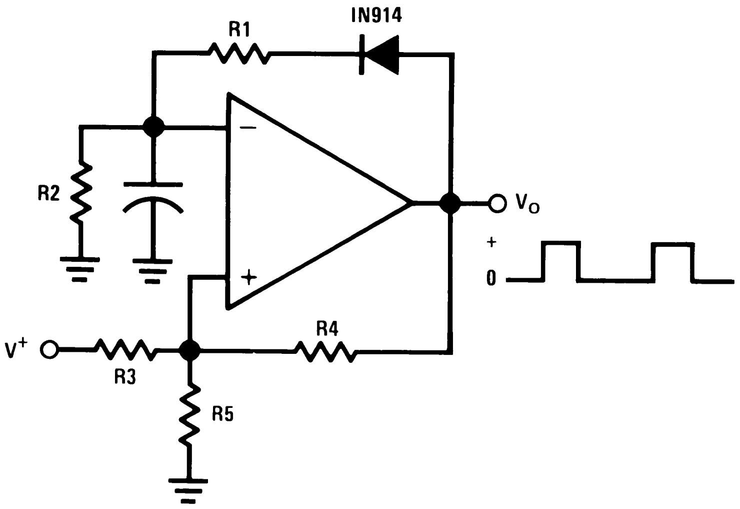


Figure 21. Pulse Generator

Figure 22 is a squarewave generator with the same path for charging and discharging the capacitor.

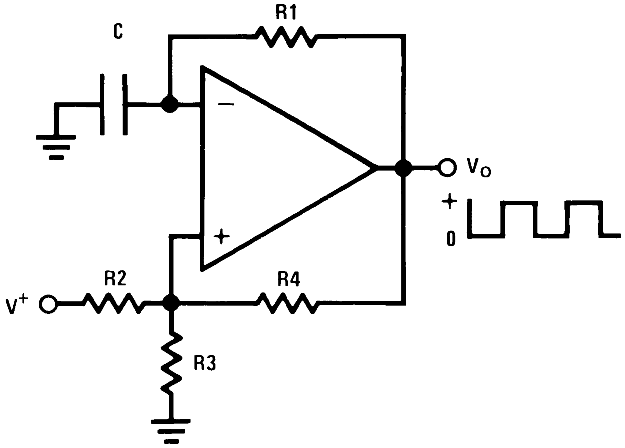


Figure 22. Squarewave Generator

CURRENT SOURCE AND SINK

The LMV321/LMV358/LMV324 can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks.

Fixed Current Source

A multiple fixed current source is shown in Figure 23. A voltage (V_{REF} = 2V) is established across resistor R_3 by the voltage divider (R_3 and R_4). Negative feedback is used to cause the voltage drop across R_1 to be equal to V_{REF}. This controls the emitter current of transistor Q_1 and if we neglect the base current of Q_1 and Q_2, essentially this same current is available out of the collector of Q_1.

Large input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the β of Q_1.

The resistor, R_2, can be used to scale the collector current of Q_2 either above or below the 1 mA reference value.

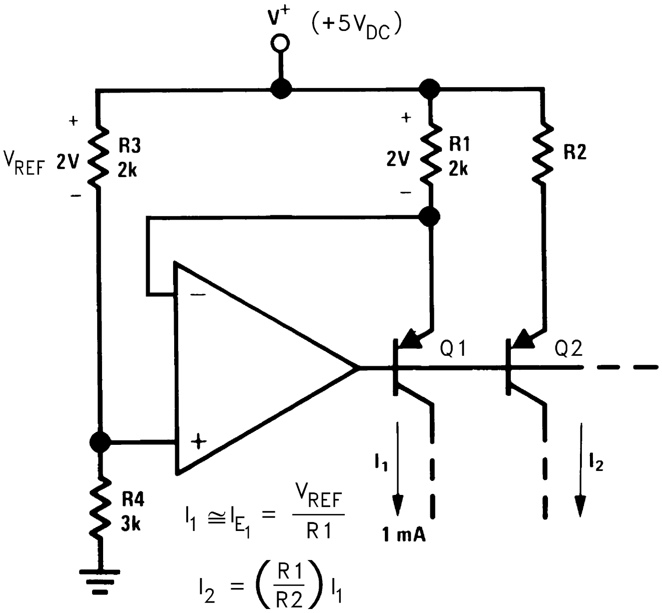

V^+ $(+5V_{DC})$
+
V_{REF} 2V
–
R3
2k
+
2V
–
R1
2k
R2
–
+
Q1
Q2
I_1
I_2
1 mA
R4
3k
$I_1 \cong I_{E_1} = \frac{V_{REF}}{R1}$
$I_2 = \left(\frac{R1}{R2}\right) I_1$

Figure 23. Fixed Current Source

High Compliance Current Sink

A current sink circuit is shown in Figure 24. The circuit requires only one resistor (R_E) and supplies an output current which is directly proportional to this resistor value.

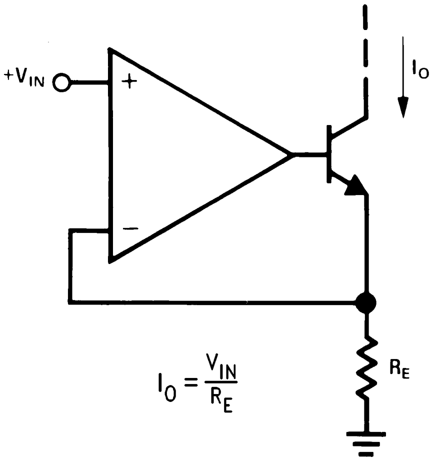


Figure 24. High Compliance Current Sink

POWER AMPLIFIER

A power amplifier is illustrated in Figure 25. This circuit can provide a higher output current because a transistor follower is added to the output of the op amp.

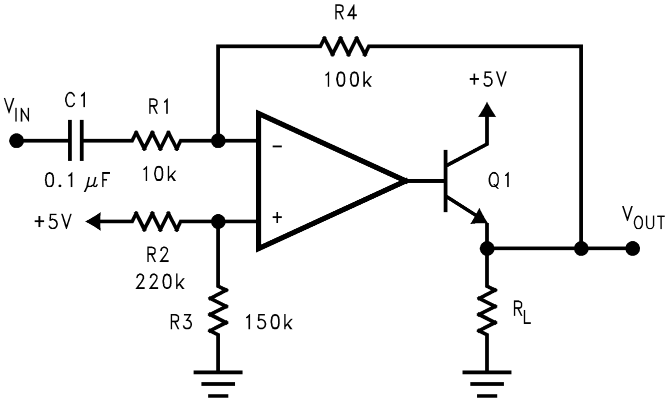


Figure 25. Power Amplifier

LED DRIVER

The LMV321/LMV358/LMV324 can be used to drive an LED as shown in Figure 26.

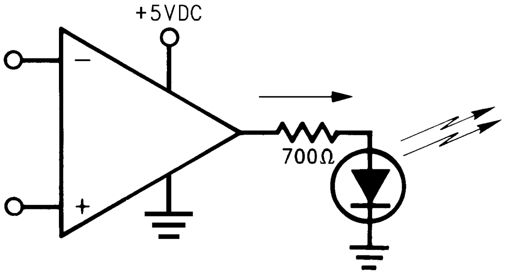


Figure 26. LED Driver

COMPARATOR WITH HYSTERESIS

The LMV321/LMV358/LMV324 can be used as a low power comparator. Figure 27 shows a comparator with hysteresis. The hysteresis is determined by the ratio of the two resistors.

$$V_{TH+} = V_{REF}/(1+R_1/R_2)+V_{OH}/(1+R_2/R_1) \quad (34)$$

$$V_{TH-} = V_{REF}/(1+R_1/R_2)+V_{OL}/(1+R_2/R_1) \quad (35)$$

$$V_H = (V_{OH}-V_{OL})/(1+R_2/R_1) \quad (36)$$

where

V_{TH+}: Positive Threshold Voltage

V_{TH-}: Negative Threshold Voltage

V_{OH}: Output Voltage at High

V_{OL}: Output Voltage at Low

V_H: Hysteresis Voltage

Since LMV321/LMV358/LMV324 have rail-to-rail output, the (V_{OH}-V_{OL}) is equal to V_S, which is the supply voltage.

$$V_H = V_S/(1+R_2/R_1) \quad (37)$$

The differential voltage at the input of the op amp should not exceed the specified absolute maximum ratings. For real comparators that are much faster, we recommend you use Texas Instruments's LMV331/LMV93/LMV339, which are single, dual and quad general purpose comparators for low voltage operation.

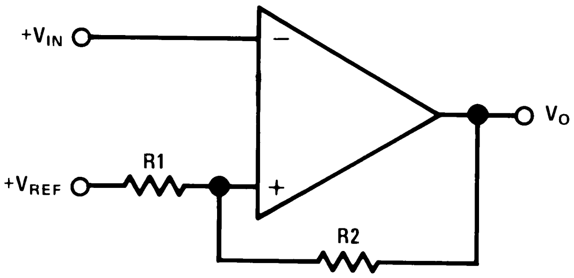


Figure 27. Comparator with Hysteresis

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV321M5	ACTIVE	SOT-23	DBV	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV321M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
LMV321M5X	ACTIVE	SOT-23	DBV	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV321M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	
LMV321M7	ACTIVE	SC70	DCK	5	1000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV321M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV321M7X	ACTIVE	SC70	DCK	5	3000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV321M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV324M	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV324M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV324MT	ACTIVE	TSSOP	PW	14	94	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV324MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV324MTX	ACTIVE	TSSOP	PW	14	2500	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV324MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV324MX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV324MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV358M	ACTIVE	SOIC	D	8	95	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV358M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV358MM	ACTIVE	VSSOP	DGK	8	1000	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV358MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LMV358MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	CU SNPB	Level-1-260C-UNLIM	
LMV358MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LMV358MX	ACTIVE	SOIC	D	8	2500	TBD	CU SNPB	Level-1-235C-UNLIM	
LMV358MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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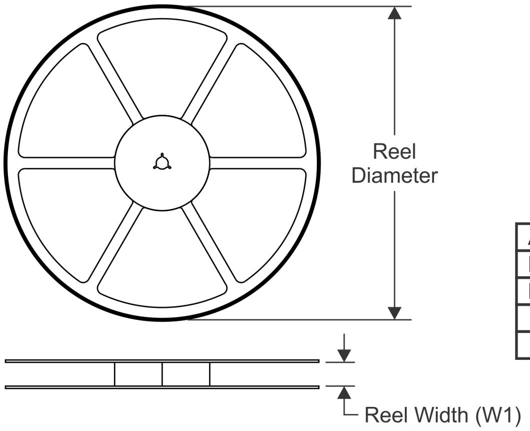
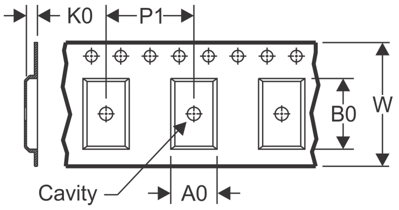
TAPE AND REEL INFORMATION

REEL DIMENSIONS

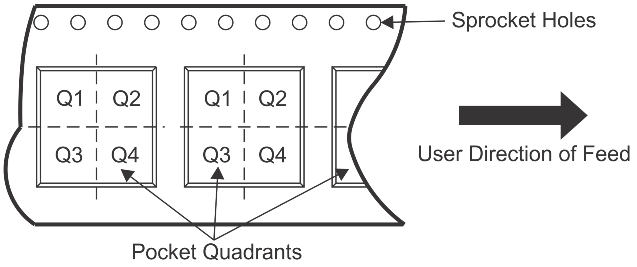


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

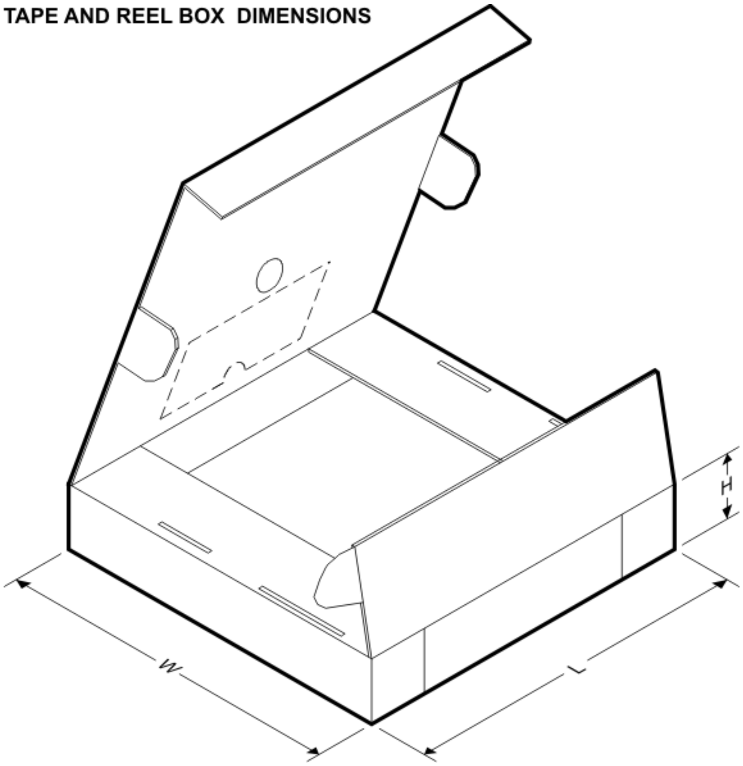
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV321M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV321M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV321M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV321M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV321M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV324MTX	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV324MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LMV324MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV324MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV358MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV358MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

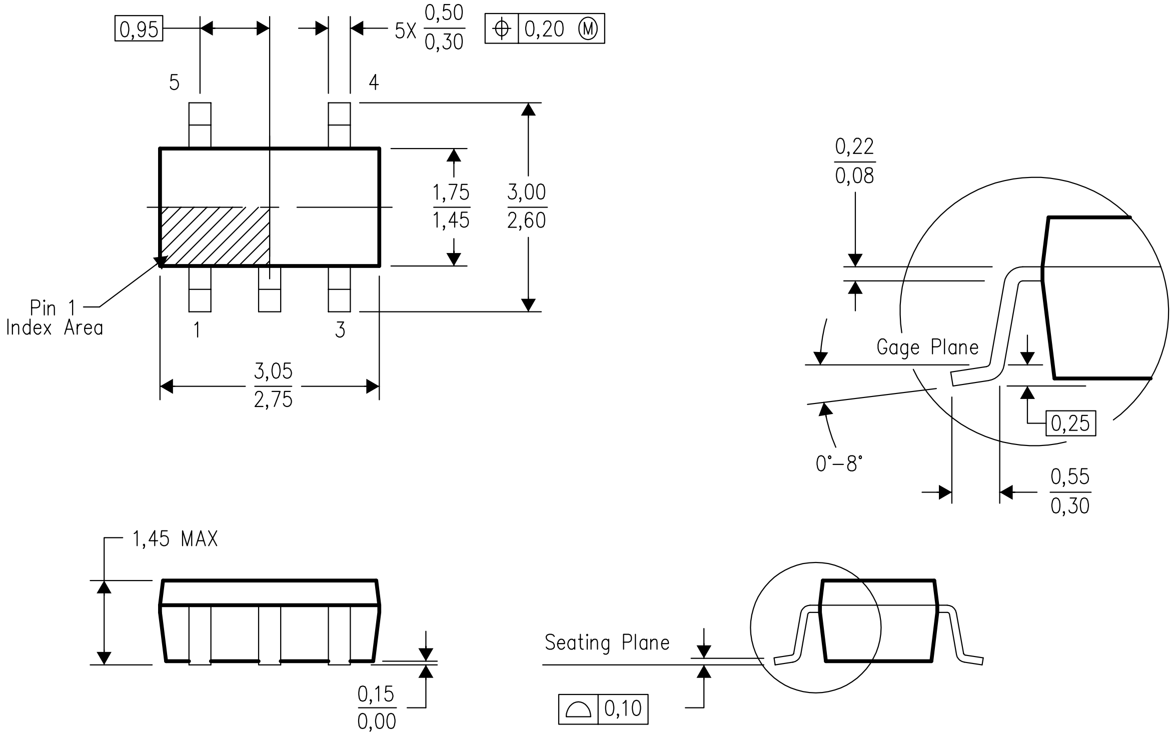
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV321M5	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV321M5/NOPB	SOT-23	DBV	5	1000	203.0	190.0	41.0
LMV321M5X	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV321M5X/NOPB	SOT-23	DBV	5	3000	206.0	191.0	90.0
LMV321M7	SC70	DCK	5	1000	203.0	190.0	41.0
LMV321M7/NOPB	SC70	DCK	5	1000	203.0	190.0	41.0
LMV321M7X	SC70	DCK	5	3000	206.0	191.0	90.0
LMV321M7X/NOPB	SC70	DCK	5	3000	206.0	191.0	90.0
LMV324MTX	TSSOP	PW	14	2500	349.0	337.0	45.0
LMV324MTX/NOPB	TSSOP	PW	14	2500	349.0	337.0	45.0
LMV324MX	SOIC	D	14	2500	349.0	337.0	45.0
LMV324MX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0
LMV358MM	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV358MM/NOPB	VSSOP	DGK	8	1000	203.0	190.0	41.0
LMV358MMX	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV358MMX/NOPB	VSSOP	DGK	8	3500	349.0	337.0	45.0
LMV358MX	SOIC	D	8	2500	349.0	337.0	45.0
LMV358MX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

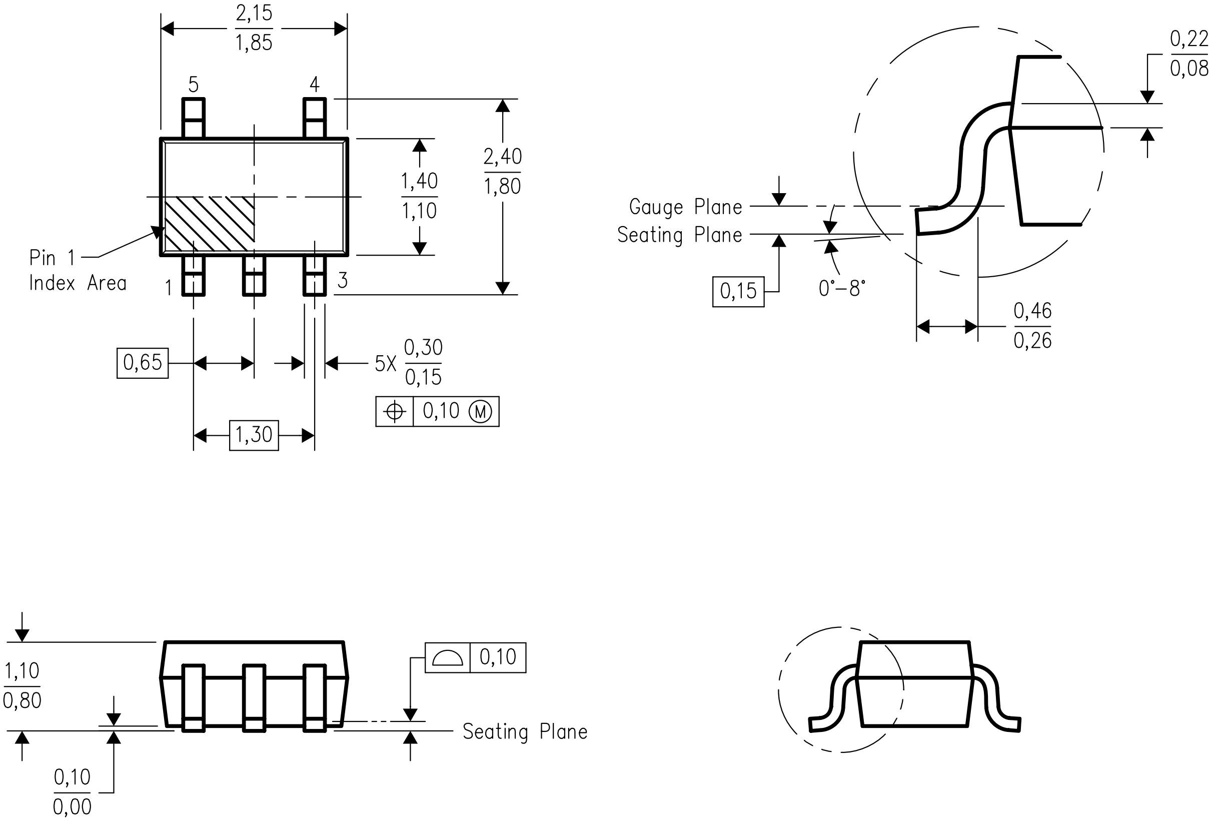
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE


0,95
5X 0,50 / 0,30
0,20 M
5
4
1,75 / 1,45
3,00 / 2,60
Pin 1 Index Area
1
3
3,05 / 2,75
0,22 / 0,08
Gage Plane
0,25
0°–8°
0,55 / 0,30
1,45 MAX
0,15 / 0,00
Seating Plane
0,10

4073253–4/K 03/2006

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO–178 Variation AA.

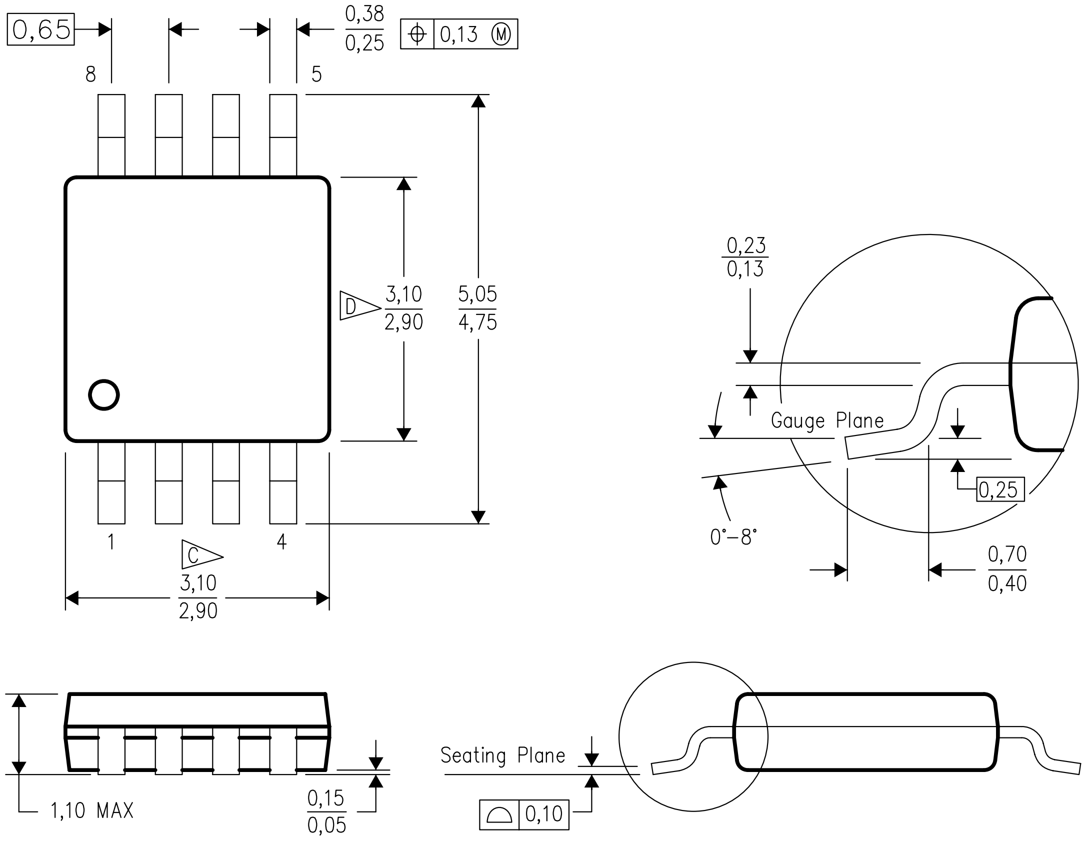
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE


2,15
1,85
5
4
2,40
1,80
1,40
1,10
Pin 1
Index Area
1
3
0,65
5X 0,30
0,15
⌖ 0,10 Ⓜ
1,30
0,22
0,08
Gauge Plane
Seating Plane
0,15
0°–8°
0,46
0,26
1,10
0,80
0,10
0,00
⌓ 0,10
Seating Plane

4093553-3/G 01/2007

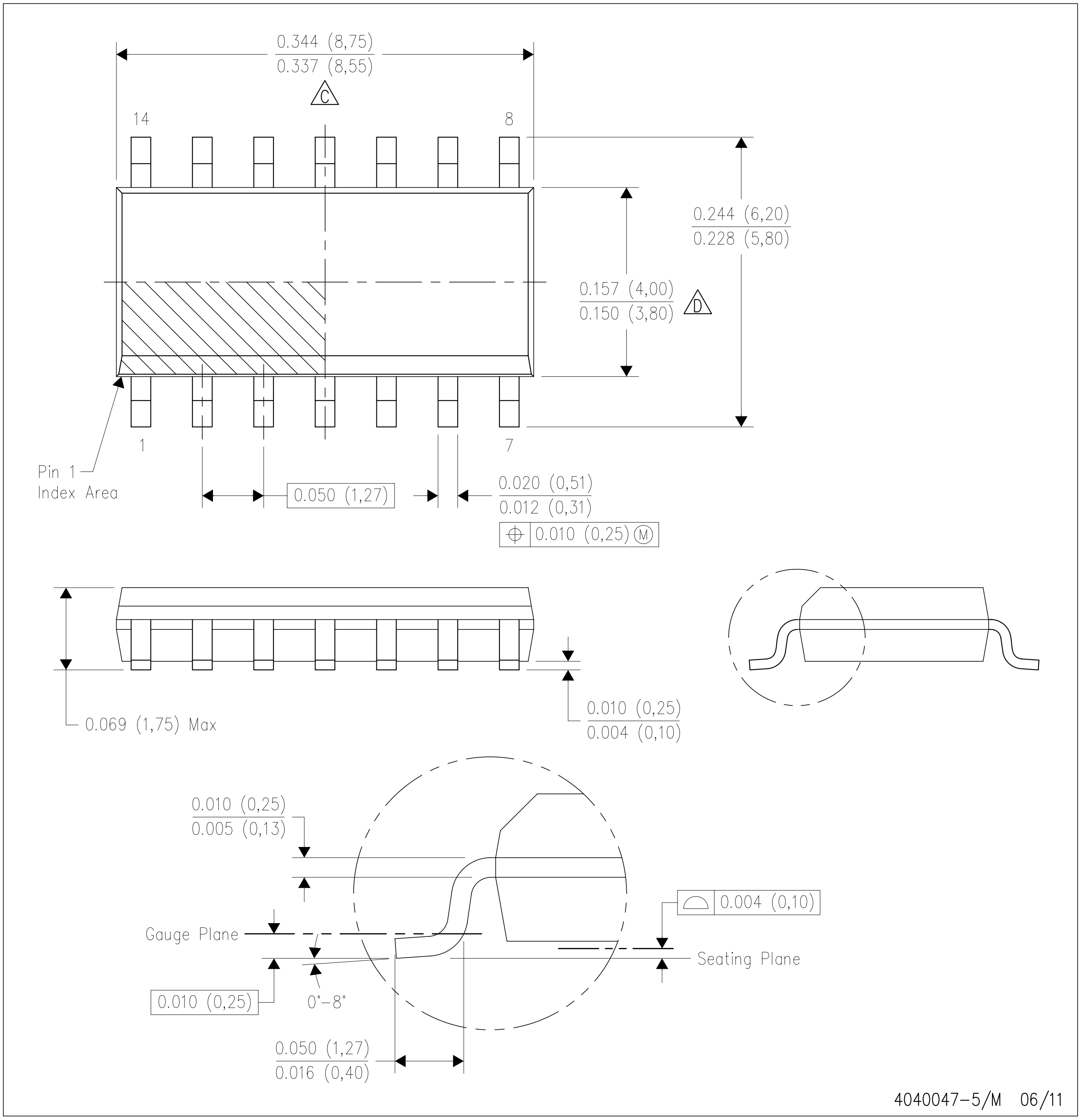
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE


0,65
0,38
0,25
0,13 Ⓜ
8
5
3,10
2,90
5,05
4,75
D
1
4
C
3,10
2,90
0,23
0,13
Gauge Plane
0,25
0°–8°
0,70
0,40
1,10 MAX
0,15
0,05
Seating Plane
0,10
4073329/E 05/06

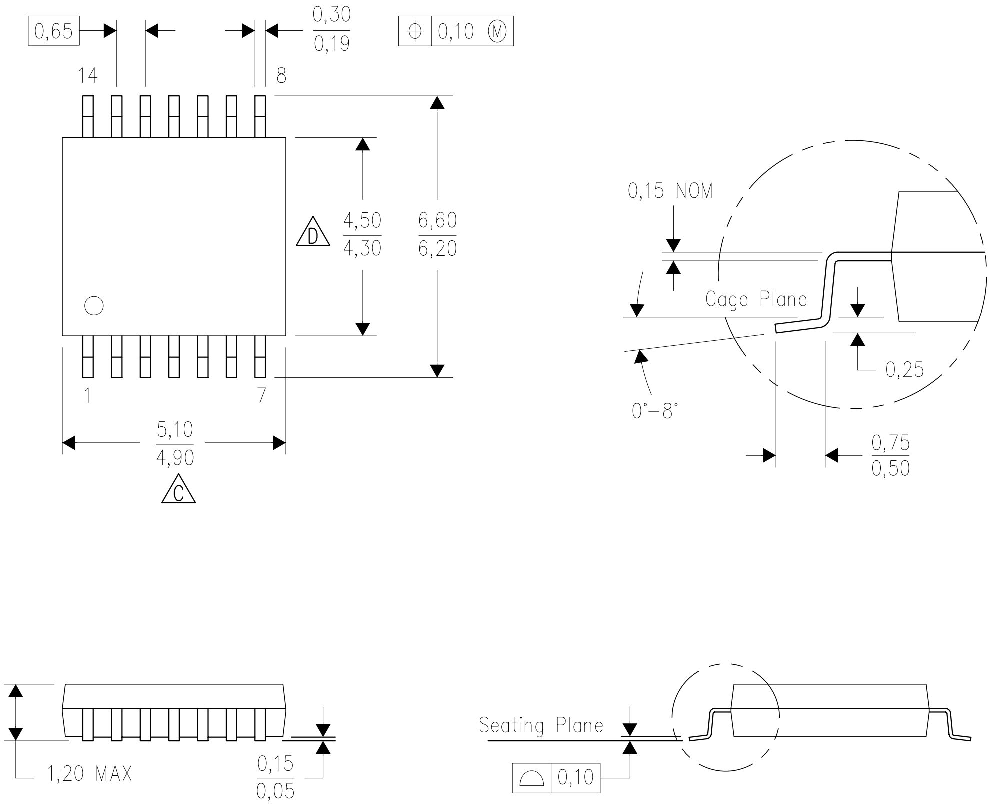
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE


0.344 (8,75)
0.337 (8,55)
△C
14
8
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
△D
1
7
Pin 1
Index Area
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
⌖ 0.010 (0,25) Ⓜ
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.010 (0,25)
0°–8°
0.004 (0,10)
Seating Plane
0.050 (1,27)
0.016 (0,40)
4040047–5/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

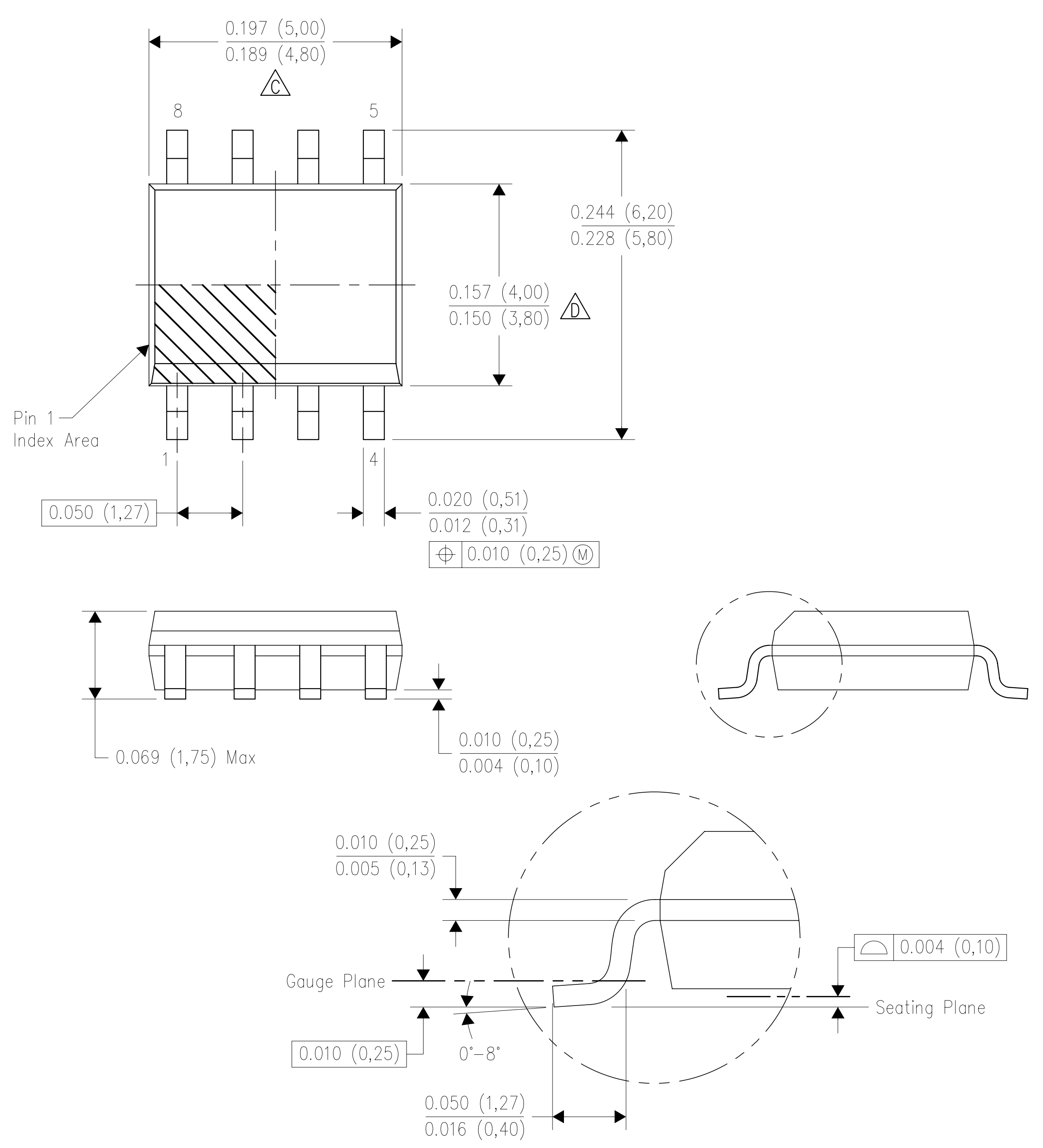
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE


0,65
0,30
0,19
⌖ 0,10 Ⓜ
14
8
1
7
D
4,50
4,30
6,60
6,20
5,10
4,90
C
0,15 NOM
Gage Plane
0,25
0°–8°
0,75
0,50
1,20 MAX
0,15
0,05
Seating Plane
⌓ 0,10

4040064–3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

D (R-PDSO-G8) PLASTIC SMALL OUTLINE


0.197 (5,00)
0.189 (4,80)
C
8
5
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
Pin 1 Index Area
1
4
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.004 (0,10)
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

4040047-3/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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